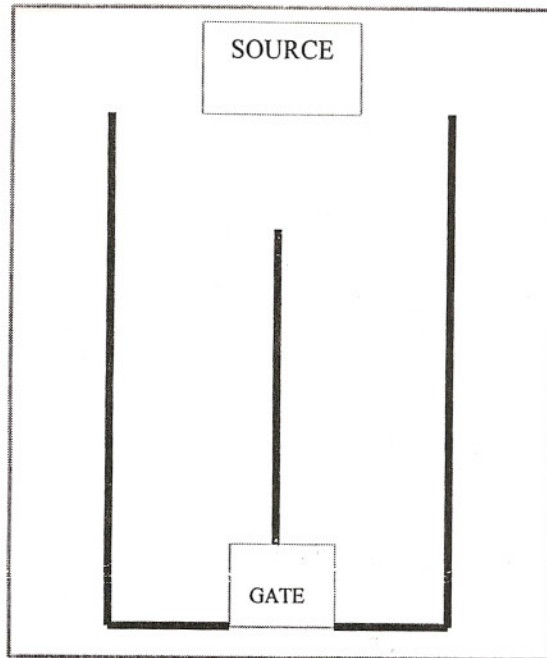




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



GATE PAD: 0.016 X 0.026; SOURCE PAD: 0.034 X 0.025;

Topside Metal: Al
Backside: CrNiAg
Backside Potential: Drain
Mask Ref:
Bond Pads: .004" min

APPROVED BY: CB
MFG: IRI

DIE SIZE: .116" x .181"
THICKNESS: .016"

DATE: 2/8/01
P/N: IRFC9230

DG 10.1.2
Rev A 3-4-99